Tektronix

Technical Brief

Probing High Frequency Digital Circuitry

"Are you failing good circuits with the wrong probe?"

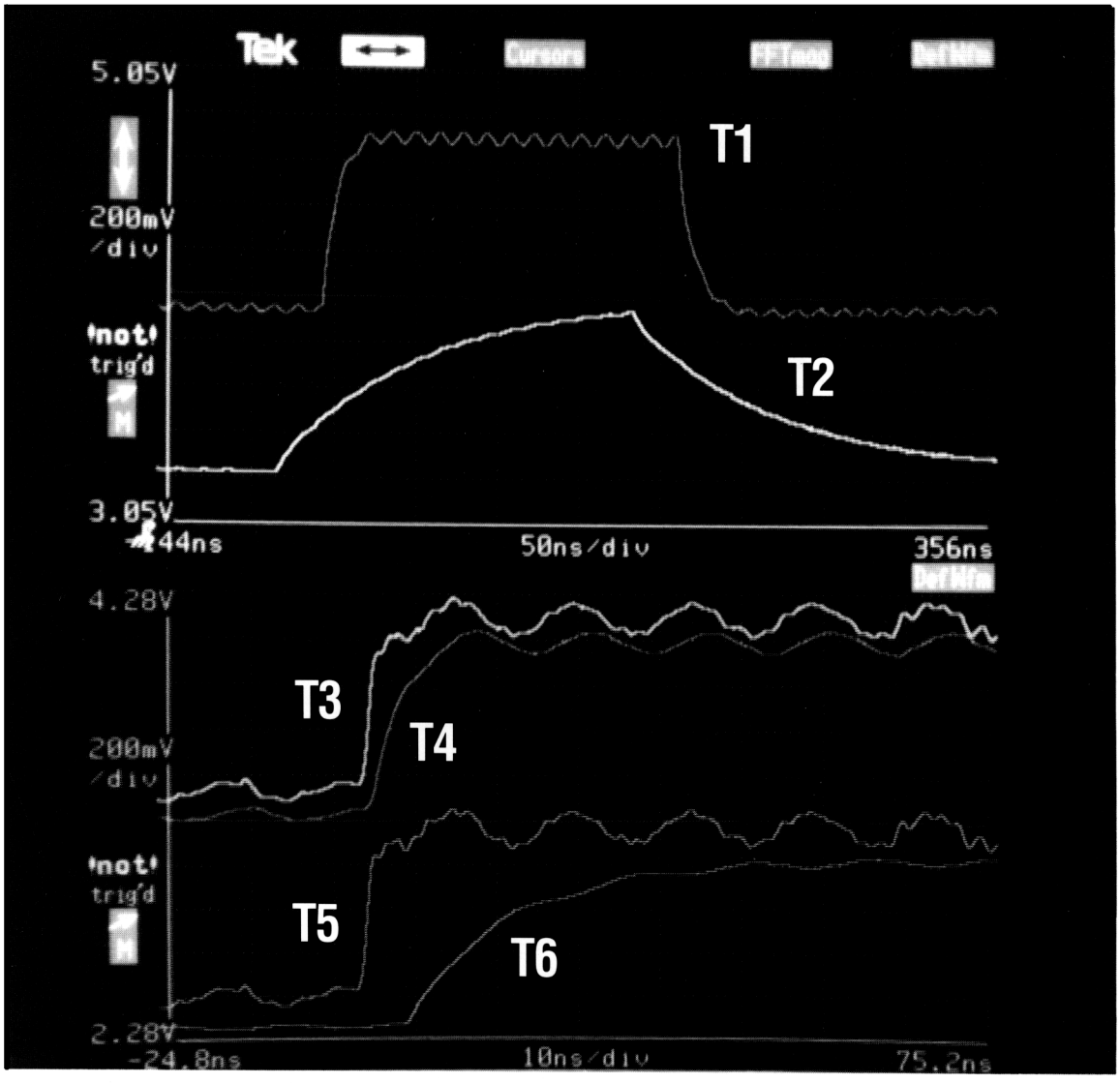

Figure 1. The above waveforms show impedance points of 50 ohms and 1k ohms as probed with a 1X Passive probe [Trace T1 (50 Ω), Trace T2 (1 kΩ)], a 10X Active FET probe [Trace T3 (50 Ω), Trace T4 (1 kΩ)] and a 10X Passive probe [Trace T5 (50 Ω), Trace T6 (1 kΩ)].

Your signal measurement results can only be as accurate as the test and measurement tools you use. As clock rates and edge speeds of today's electronic circuits increase, probing becomes a critical piece of the measurement system – that component of your test system that comes in direct contact with your circuit. Using a probe that is not designed for high-speed applications can introduce measurement errors, resulting in costly delays.

The ideal probe/oscilloscope combination should acquire your signal and truly represent it without unduly loading or otherwise changing the signal source. In today's high-speed environments, digital designers are turning to high performance Active FET probes to reduce device under test (DUT) loading, thus providing more accurate rise time, propagation delay, aberration and amplitude measurements.

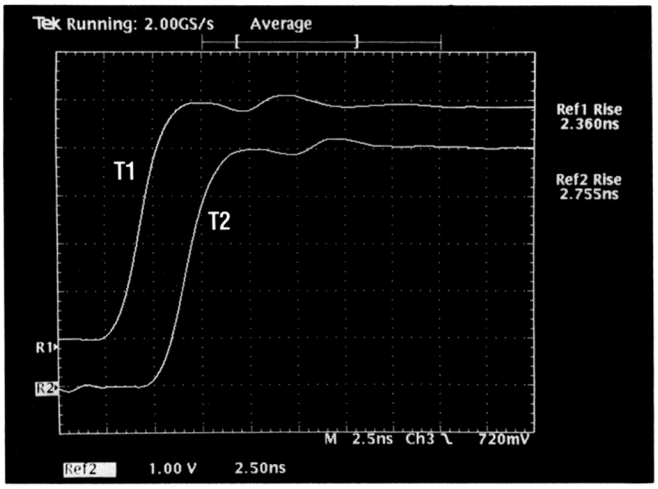

Figure 2. Probing a CMOS Inverter Circuit with a Passive Probe and an Active FET Probe.

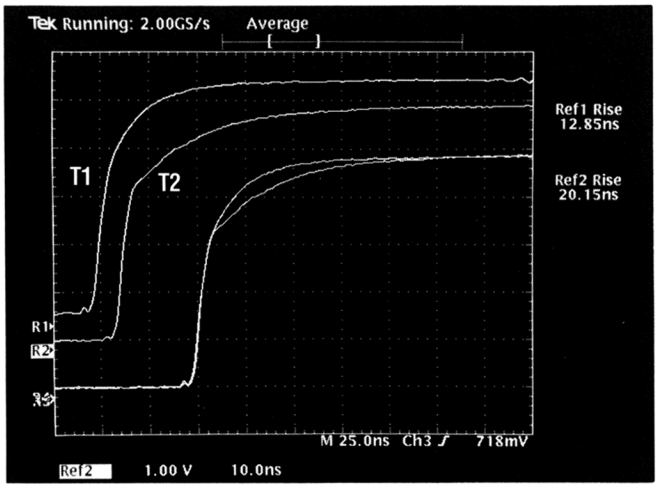

Figure 3. Probing a LSTTL Inverter (Open Collector) Circuit with a Passive Probe and an Active FET Probe.

CMOS Inverter Circuit Data for Figure 2

Logic Family Device	Rise Time (ns) P6139A - Passive (8 pF / 10 MΩ)	Rise Time (ns) P6205 - Active FET (2 pF / 1 MΩ)	Conclusion
CMOS Inverter Output	2.76 (Trace T2)	2.36 (Trace T1)	Passive probe capacitance loads device output

LSTTL Inverter (Open Collector) Circuit Data for Figure 3

Logic Family Device	Rise Time (ns) P6139A - Passive (8 pF / 10 MΩ)	Rise Time (ns) P6205 - Active FET (2 pF / 1 MΩ)	Conclusion
LSTTL (Open Collector)	20.15 (Trace T2)	12.85 (Trace T1)	Passive probe capacitance loads device output

Device Technology. TTL, CMOS, ECL, and GaAs circuit designs each present unique challenges when high speed signal acquisition is required. Each of the more common digital logic families exhibit their own idiosyncrasies as we try to squeeze more speed from them. The challenges presented by modern device technologies require digital designers to employ high speed analog design techniques such as: amplifier line drivers, strip lines, and impedance matching.

CMOS and TTL circuits are especially sensitive to capacitive loading of their outputs. The rate at which the output voltage can swing is a function of the device topology and current sourcing or sinking capability, the device output source resistance, and the combined impedances of all the loads attached to the output. To minimize the probe's contribution to this effect, you should use a probe with as little capacitive and resistive loading as possible.

For example, a CMOS inverter with its output connected to the input of a single CMOS device might be expected to operate at maximum speed, as the capacitive loading related to fan-out is minimized (see Figure 2). A device in this configuration was probed using a P6205 10X Active FET probe (Trace T1) and a P6139A 10X Passive probe (Trace T2).

Some device technologies, such as ECL and Low-power Schottky TTL have non-saturating output stages which are able to provide more current to charge load capacitances than saturating logic families are capable of. However, probe capacitive loading still has a detrimental effect upon circuit operation. Even when you do not see a change while probing, more than likely circuit changes are occurring. A Schottky TTL open-collector inverter, with its output connected through 1 kΩ to the +5 volt supply was probed with a P6205 10X Active FET probe (Figure 3, Trace T1) and a P6139A 10X Passive probe (Figure 3, Trace T2). (Note: The Trace shown at the bottom of the photo in Figure 3 is an overlay of Traces T1 and T2.)

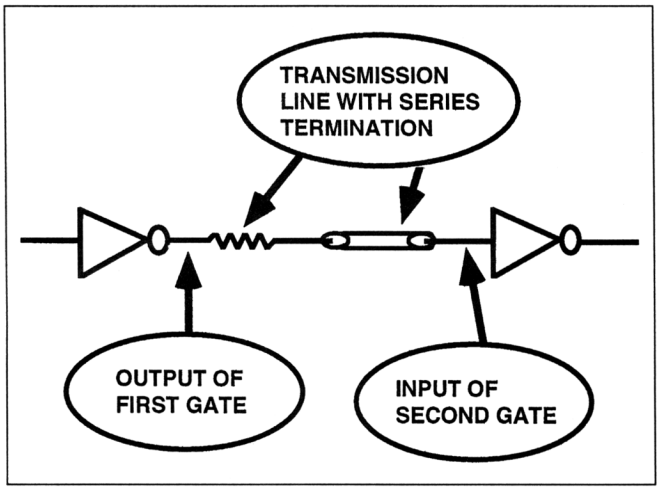

Figure 4a. Test Setup for Probing the Output and Input of a Device with a Series Termination using a Passive Probe and an Active FET Probe.

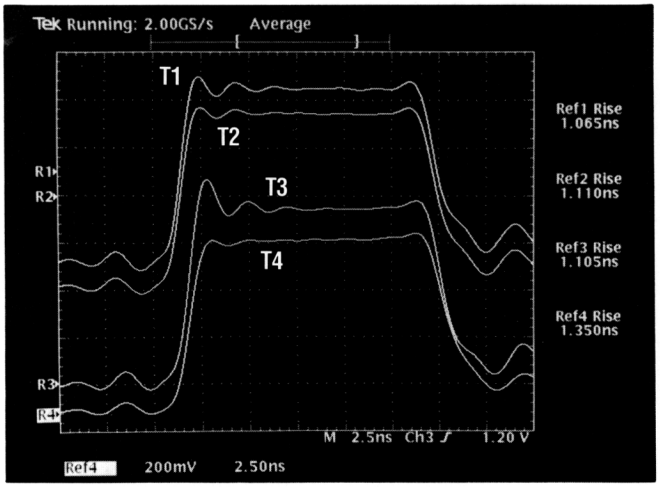

Figure 4b. Probing an ECL Circuit with Series Termination with a Passive Probe and an Active FET Probe.

ECL Circuit with Series Termination Data for Figure 4b

Logic Family Device	Rise Time (ns) P6139A - Passive (8 pF / 10 MΩ)	Rise Time (ns) P6205 - Active FET (2 pF / 1 MΩ)	Conclusion
ECL Output	1.11 (Trace T3)	1.07 (Trace T1)	Passive probe capacitive loading slows transmission line rise time
ECL Next Stage Input	1.35 (Trace T4)	1.11 (Trace T2)	

Table 1. LSTTL & CMOS Circuits with Series Termination Data Only (No Photo)

Logic Family Device	Rise Time (ns) P6139A - Passive (8 pF / 10 MΩ)	Rise Time (ns) P6205 - Active FET (2 pF / 1 MΩ)	Conclusion
LSTTL Output	3.94	3.81	
LSTTL Next Stage Input	4.94	3.86	
CMOS Output	2.73	2.38	Passive probe capacitive loading slows transmission line rise time
CMOS Next Stage Input	3.42	2.45	

High speed device data books advise designers to consider the effects of circuit board and interconnect designs upon signal fidelity and operation. Devices which produce fast edges can generate large reflections when circuit board trace impedances are uncontrolled. Such reflections can cause such problems as data errors, reduced noise immunity, and decreased immunity to power supply variations. These problems can be greatly reduced by designing controlled-impedance circuit board runs terminated in an impedance equal to Zo.

ECL, CMOS, and LSTTL devices were tested in circuits involving series terminated lines (see Figure 4a above). Rise time measurements were made at the output of an ECL device (Figure 4b, Trace T1 with a P6205 10X Active FET probe and Trace T3 with a P6139A 10X Passive probe) and then were compared with those made at the input to the next stage (Figure 4b, Trace T2 with a P6205 10X Active FET probe and Trace T4 with a P6139A 10X Passive probe). Table 1 shows the same measurements taken from LSTTL and CMOS logic devices.

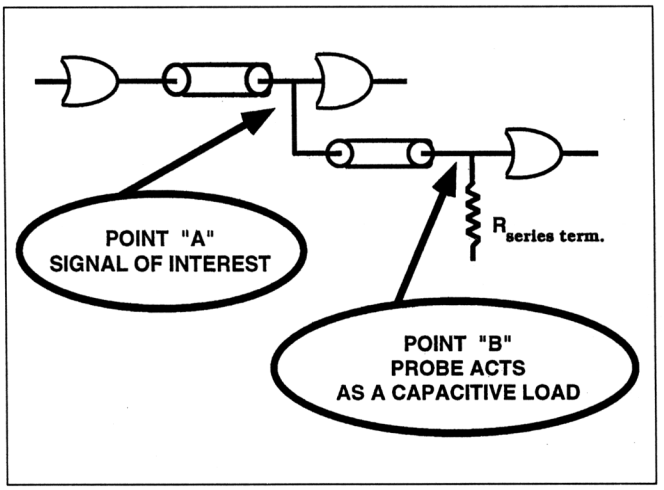

Figure 5a. Test Setup for Probing an ECL Transmission Line In a Daisy Chain Configuration.

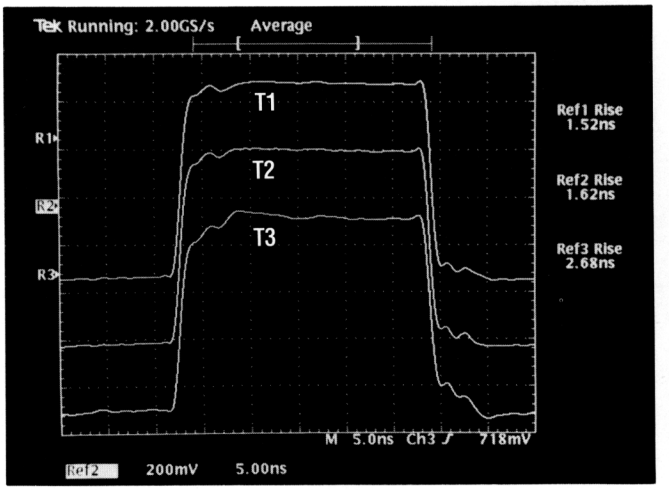

Figure 5b. Probing an ECL Circuit with Daisy Chained Transmission Line with a Passive Probe and an Active FET Probe.

ECL Daisy Chain Transmission Line Data for Figure 5

	Rise Time (ns)		
	Probe Type Probing Point "A"		
Logic Family Device	**P6139A - Passive (8 pF / 10 MΩ)**	**P6205 - Active FET (2 pF / 1 MΩ)**	**Conclusion**
Probing point "B" with a Passive probe load at the input to the next gate while probing point "A" as indicated	4.14 (Not shown)	2.68 (Trace T3)	
Probing pioint "B" with an Active FET probe load at the input to the next gate while probing point "A" as indicated	2.14 (Not shown)	1.62 (Trace T2)	Passive probe load on transmission line disturbs devices upstream
Probing point "B" with no probe load at the input to the next gate while probing point "A" as indicated	2.04 (Not shown)	1.52 (Trace T1)	

In another test, the output of an ECL gate was connected to two ECL inputs using 50 Ω cables in a daisy chain arrangement simulating long transmission lines, with the 50 Ω parallel termination resistor connected at the end of the chain (see Figure 5a).
Figure 5b shows three waveforms acquired at point "A" with a P6205 10X Active FET probe. Trace T1 shows the waveform at point "A" when no probe is attached to point "B". Trace T2 shows the waveform at point "A" while a P6205 10X Active FET probe is attached to point "B". Trace T3 shows the waveform at point "A" while a P6139A 10X Passive probe is attached to point "B". Figure 5b's Table also includes measurements made with a P6139A 10X Passive probe attached to point "A" using the same sequence of probes attached to point "B".

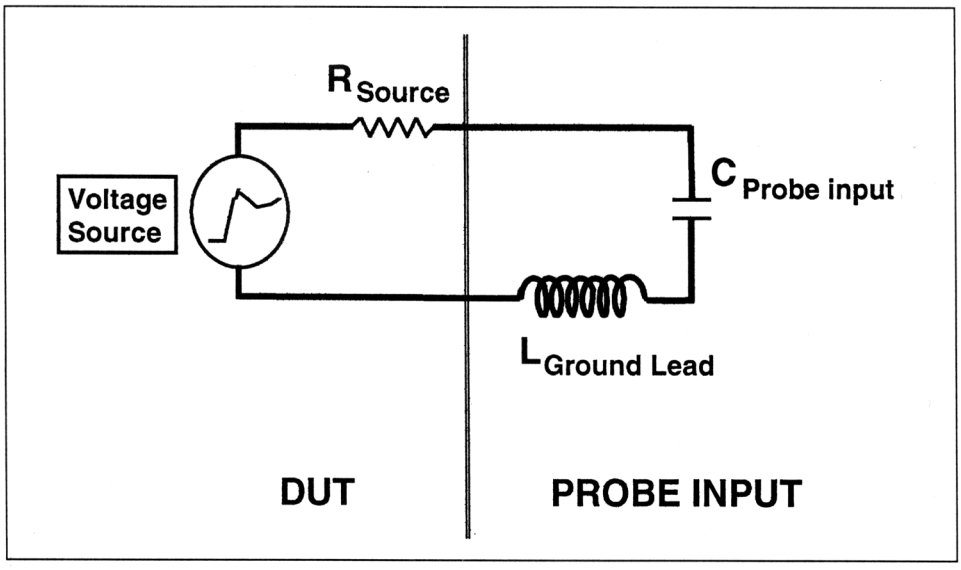

Figure 6. Probe with Ground Lead Equivalent Circuit.

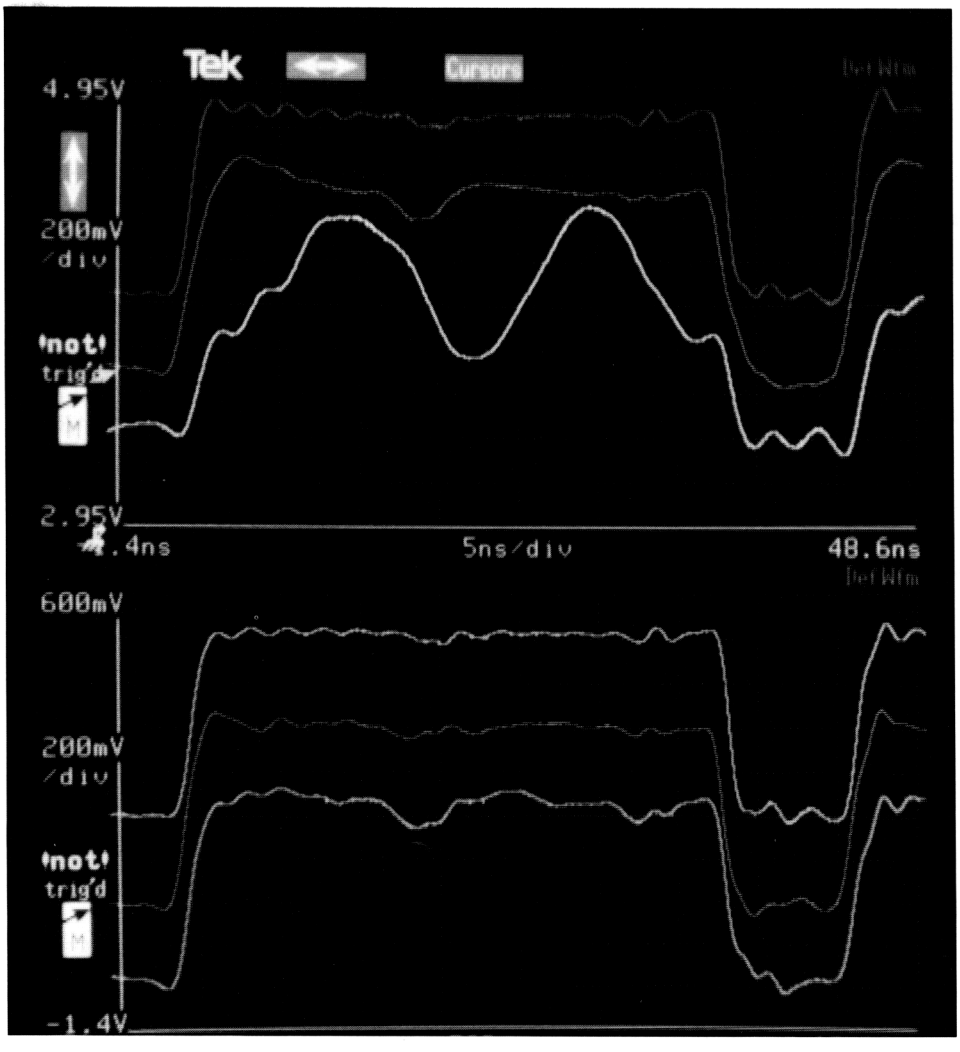

Figure 7. The Effects of Probe Ground Lead Inductance.

Ground Lead Inductance. All of the measurements described in Figures 1 thru 5 were made using very short probe grounding adapters, which improves the measurement capability of any voltage probe. Many applications require the use of a longer ground lead due to the lack of local access to circuit ground. However, the inductance associated with longer ground leads can adversely effect the accuracy of your measurements.

A ground lead is a wire that provides a local ground-return path when you are measuring any signal. An inadequate ground lead (one that is too long) can reduce the fidelity of the high frequency portion of the displayed signal.

When making any kind of absolute measurement, such as amplitude, rise time, or propagation delay, you should use the shortest grounding path possible. Why? Because the ground lead inductance and the probe's input capacitance form a series resonant circuit which rings when excited by a fast pulse (see Figure 6).

Figure 7 shows the output waveform of an ECL counter acquired using a variety of probe-ground lead combinations. The top three traces show how the displayed waveform changes as the Passive probe's ground lead length is increased from less than 1/2 inch (top trace) to 6 inches to 12 inches (bottom trace). The bottom three traces show how the Active FET probe waveform remains relatively unchanged regardless of ground lead length using the same ground lead sequence as before. The additional inductance of a long ground lead is more likely to introduce aberrations in a Passive probe than an Active FET probe.

Conclusion. At high speeds, the probe you select for your measurements can critically affect your test results. Capacitive loading becomes increasingly important as frequency increases. Source impedance and ground lead length also become significant factors. Both Passive and Active FET probes have their place. The wide dynamic range of passive probes allows them the versatility of making low and medium frequency measurements at moderately high voltages. However, the input capacitance of passive probes limits their effectiveness at high speeds by capacitively loading the DUT and introducing ringing in the circuit when used with long ground leads. Active probes are ideal for high speed design because of their lower input capacitance and wider useful bandwidth. An active probe, coupled with a wide bandwidth, multi-channel oscilloscopes, like the TDS600 or DSA600 series, gives the digital designer the measurement tools required by today's technologies.

Additional Reading Material:

ABC's Of Probes
Tektronix, Inc.
Literature # 60W-6053-4

High Speed Amplifier Techniques
A Designer's Companion for Wideband Circuitry
Application Note 47, August 1991
Linear Technology Corporation
Literature # AN47-132
Phone: (408) 432-1900
FAX: (408) 434-0507

Active Probes:
Their Unique Characteristics and Applications
Tektronix, Inc.
Literature # 60W-6883

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